Appl. No. 10/787,444
Amdt. dated June 23, 2006
Reply to Office action of March 27, 2006

REMARKS

Receipt of the Office action dated March 27, 2006, is hereby acknowledged. In that action the Examiner rejected all the claims as allegedly anticipated by Herring et al. (U.S. Pat. No. 5,860,081, hereinafter "Herring").

I. SECTION 102 REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). Herring's Figure 1 is reproduced below for convenience of the discussion.

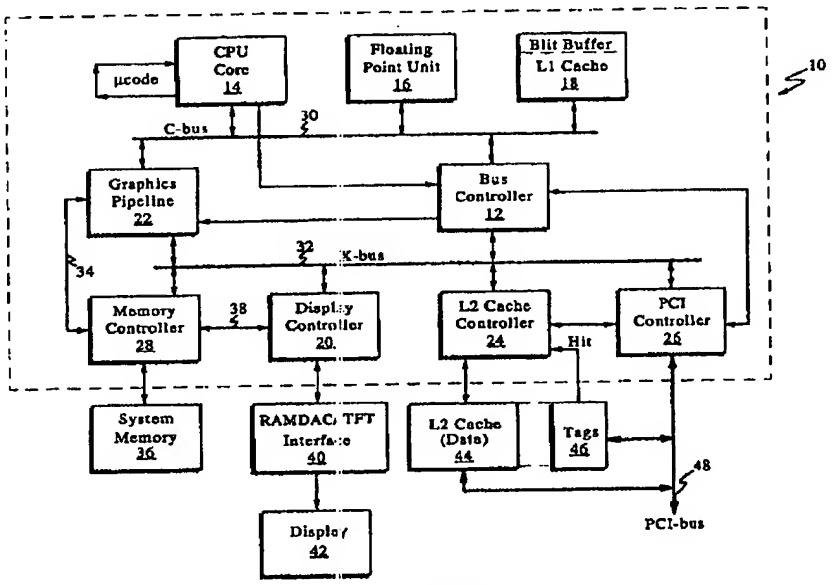

FIG. 1

In Herring, both the L2 cache controller 24 and the PCI controller 26 are disposed within the CPU 10.

> The CPU 10 includes the following functional units: an internal bus controller 12, a CPU core 14, a (level-two) L2 cache controller 24, a PCI-bus controller 26...

(Herring Col. 4, lines 15-18). So that a separate CPU bus need not be available external to the CPU, both the L2 cache controller 24 and the peripheral bus controller 26 utilize the same external bus 48.

> [T]he present invention discloses a highly integrated central processing unit having L2 cache support employing **a time-multiplexed, on-demand bus**, separate from the CPU bus, **to support both a high performance L2 cache as well as other peripherals** ... . An **integrated** L2 cache controller and local bus controller cooperate to support different protocols depending on whether L2 cache or local bus operating is required.

(Herring Col. 2, lines 44-52 (emphasis added)).

Claim 1, by contrast, specifically recites, "a central processing unit ("CPU"); a bridge device coupled to a main memory; a cache controller coupled between the bridge device and the CPU; and a cache memory coupled to the cache controller and providing cache memory space to the CPU ... ." The Office action relies on Herring's PCI controller 26 as the claimed bridge device, and also relies on Herring's cache controller 24 for the claimed cache controller. Even if hypothetically one ignores the fact that Herring's controllers 24 and 26 are expressly part of the highly integrated CPU 10 (which Applicant does not admit is proper), Herring does not expressly or inherently teach that the cache controller 24 could or should couple between Herring's CPU core 14 and Herring's PCI controller 26. In fact, it appears that the cache controller 24 and the PCI controller 26 are peers on the X-bus 32. For this reason alone the rejection should be withdrawn.

Claim 1 further recites, "wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using a first communication protocol and the bridge device communicates using a second communication protocol, and wherein the cache controller allows communication between the CPU and the bridge device when the CPU communicates using the second communication protocol and the bridge device communicates using the first communication protocol." Herring's cache controller 24 does not allow communication on both sides of the cache controller

to implement the claimed multiple protocols. For example, Herring does not expressly or inherently teach using a first and second communication protocols on the X-bus 32.

Based on the foregoing, Applicant respectfully submits that claim 1 is not anticipated by Herring, and should be allowed together with all claims which depend from claim 1 (claims 2-4).

B. Claim 5

Claim 5 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). In particular, Herring discloses a highly integrated central processing unit where a general purpose peripheral interface (*e.g.*, PCI bus) is used both an interface bus to peripherals and as a mechanism to communicate with L2 cache. (Herring Abstract). The L2 cache controller in Herrings "highly integrated circuit" is disposed within the CPU 10. (Herring Col. 4, lines 15-18).

Claim 5, by contrast, specifically recites, "A cache controller, comprising: a first interface operable to communicate to an external device using a first communication protocol; a second interface operable to communicate to an external device using a second communication protocol different than the first communication protocol; and a cache memory interface coupled to the first and second interfaces ... ." In the Herring system, the external (to the CPU 10) device to which the cache controller 24 couples is the L2 cache. Thus, Herring does not expressly or inherently teach "first interface operable to communicate to an **external** device using a first communication protocol; a second interface operable to communicate to an **external** device using a second communication protocol different than the first communication protocol." For this reason alone the rejection should be withdrawn.

Claim 5 further recites. "wherein the first interface selectively communicates to an external device being one of a CPU and a bridge device; wherein the second interface selectively communicates to an external device being one of a CPU and a bridge device." Even if it is hypothetically assumed

that the connection of Herring's cache controller 24 to the X-bus 32 allows communication to the core 14 and a "bridge device" (which Applicant does not admit is proper), Herring still fails to expressly or inherently teach the cache controller having a "second interface [that] selectively communicates to an external device being one of a CPU and a bridge device."

Based on the foregoing, Applicant respectfully submits that claim 5 is not anticipated by Herring, and should be allowed together with all claims which depend from claim 5 (claims 6-11).

C. Claim 12

Claim 12 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). In particular, Herring discloses a highly integrated central processing unit where a general purpose peripheral interface (*e.g.*, PCI bus) is used both an interface bus to peripherals and as a mechanism to communicate with L2 cache. (Herring Abstract). The L2 cache controller in Herrings "highly integrated circuit" is disposed within the CPU 10. (Herring Col. 4, lines 15-18).

Claim 12, by contrast, specifically recites, "configuring a first port of a cache controller to communicate to an external device, wherein the first port selectively communicates to one of a CPU and a bridge device using a first communication protocol; and configuring a second port of the cache controller to communicate to an external device, wherein the second port selectively communicates to one of a CPU and a bridge device using a second communication protocol." In the Herring system, the external (to the CPU 10) device to which the cache controller 24 couples is the L2 cache. Thus, Herring does not expressly or inherently teach "configuring a first port of a cache controller to communicate to an **external** device ... and configuring a second port of the cache controller to communicate to an **external** device ... ." For this reason alone the rejection should be withdrawn.

Moreover, even if it is hypothetically assumed that the connection of Herring's cache controller 24 to the X-bus 32 allows communication to the

core 14 and a "bridge device" (which Applicant does not admit is proper), Herring still fails to expressly or inherently teach "configuring a second port of the cache controller to communicate to an external device, wherein the second port selectively communicates to one of a CPU and a bridge device using a second communication protocol."

Based on the foregoing, Applicant respectfully submits that claim 12 is not anticipated by Herring, and should be allowed together with all claims which depend from claim 12 (claims 13-15).

D. Claim 16

Claim 16 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). In particular, Herring discloses a highly integrated central processing unit where a general purpose peripheral interface (*e.g.*, PCI bus) is used both an interface bus to peripherals and as a mechanism to communicate with L2 cache. (Herring Abstract). The L2 cache controller in Herrings "highly integrated circuit" is disposed within the CPU 10. (Herring Col. 4, lines 15-18).

Claim 16, by contrast, specifically recites, "a central processing unit ("CPU"); a bridge device coupled to a main memory; and means for reading and writing to a cache memory coupled between the CPU and the bridge device ... ." The Office action relies on Herring's PCI controller 26 as the claimed bridge device, and also relies on Herring's cache controller 24 for the claimed means for reading. Even if hypothetically one ignores the fact that Herring's controllers 24 and 26 are expressly part of the highly integrated CPU 10 (which Applicant does not admit is proper), Herring does not expressly or inherently teach that the cache controller 24 could or should couple between Herring's CPU core 14 and Herring's PCI controller 26. In fact, t appears that the cache controller 24 and the PCI controller 26 are peers on the X-bus 32. For these reasons alone the rejection should be withdrawn.

Claim 16 further recites, "wherein said means for reading and writing to the cache memory allows communication between the CPU and the bridge device

when the CPU communicates using a first communication protocol and the bridge device communicates using a second communication protocol, and allows communication between the CPU and the bridge device when the CPU communicates using the second communication protocol and the bridge device communicates using the first communication protocol." Herring's cache controller 24 does not allow communication on both sides of the cache controller to implement the claimed multiple protocols. For example, Herring does not expressly or inherently teach using a first and second communication protocols on the X-bus 32.

Based on the foregoing, Applicant respectfully submits that claim 16 is not anticipated by Herring, and should be allowed together with all claims which depend from claim 16 (claims 17-19).

E. Claim 20

Claim 20 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). In particular, Herring discloses a highly integrated central processing unit where a general purpose peripheral interface (*e.g.*, PCI bus) is used both an interface bus to peripherals and as a mechanism to communicate with L2 cache. (Herring Abstract). The L2 cache controller in Herrings "highly integrated circuit" is disposed within the CPU 10. (Herring Col. 4, lines 15-18).

Claim 20, by contrast, specifically recites, "A cache controller, comprising: a plurality of first communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a first communication protocol." The Office action relies on Herring's cache controller 24 as the claimed cache controller; however, Herrings cache controller 24 fails to teach a plurality of first communication protocol interfaces. The Office action attempts to rely on Herring's PCI controller 26 for an additional first communication protocol interface, but Herring's PCI controller 26 is clearly not part of the cache controller 24 (and in fact is construed to be a bridge device

in earlier rejections so the Office action uses conflicting interpretations of Herring). For this reason alone the rejection should be withdrawn.

Moreover, claim 20 further recites, "and a plurality of second communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a second communication protocol." If hypothetically Herring's cache controller 24 and PCI controller 26 are the claimed first communication protocol interfaces (which Applicant does not admit is proper), then Herring fails to expressly or inherently teach "a plurality of second communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a second communication protocol."

Based on the foregoing, Applicant respectfully submits that claim 20 is not anticipated by Herring, and should be allowed together with all claims which depend from claim 20 (claims 21-22).

F. Claim 23

Claim 23 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). In particular, Herring discloses a highly integrated central processing unit where a general purpose peripheral interface (*e.g.*, PCI bus) is used both an interface bus to peripherals and as a mechanism to communicate with L2 cache. (Herring Abstract). The L2 cache controller in Herrings "highly integrated circuit" is disposed within the CPU 10. (Herring Col. 4, lines 15-18).

Claim 23, by contrast, specifically recites, "wherein the cache controller allows communication between the CPU and the bridge device when the CPU and the bridge device communicate using different communication protocols, and wherein the cache controller also allows communication between the CPU and the bridge device when the communication protocols of the CPU and bridge device are reversed." Herring's cache controller 24 does not allow

communication on both sides of the cache controller to implement the claimed multiple protocols. For example, Herring does not expressly or inherently teach using a first and second communication protocols on the X-bus 32.

Based on the foregoing, Applicant respectfully submits that claim 23 is not anticipated by Herring, and should be allowed.

G. Claim 24

Claim 24 stands rejected as allegedly anticipated by Herring.

Herring is directed to interfacing an L2 cache to a single bus having alternative protocols. (Herring Title). In particular, Herring discloses a highly integrated central processing unit where a general purpose peripheral interface (*e.g.*, PCI bus) is used both an interface bus to peripherals and as a mechanism to communicate with L2 cache. (Herring Abstract). The L2 cache controller in Herrings "highly integrated circuit" is disposed within the CPU 10. (Herring Col. 4, lines 15-18).

Claim 24, by contrast, specifically recites, "a cache controller comprising a plurality of first communication protocol interfaces each allowing communication using an individual one of a plurality of communication protocols." The Office action relies on Herring's cache controller 24 as the claimed cache controller; however, Herrings cache controller 24 fails to teach a plurality of first communication protocol interfaces. The Office action attempts to rely on Herring's PCI controller 26 for an additional first communication protocol interface, but Herring's PCI controller 26 is clearly not part of the cache controller 24 (and in fact is construed to be a bridge device in earlier rejections so the Office action uses conflicting interpretations of Herring). For this reason alone the rejection should be withdrawn.

Moreover, claim 24 further recites that the cache controller has "a plurality of second communication protocol interfaces each allowing communication using an individual one of a plurality of communication protocols." If hypothetically Herring's cache controller 24 and PCI controller 26 are the claimed first communication protocol interfaces (which Applicant does not admit is proper), then Herring fails to expressly or inherently teach "a plurality of second

communication protocol interfaces that allow communication between the cache controller and at least one of a processor and a bridge device, wherein each of the processor and bridge device communicates using a second communication protocol."

Based on the foregoing, Applicant respectfully submits that claim 24 is not anticipated by Herring, and should be allowed together with all claims which depend from claim 24 (claims 25-28).

II. CONCLUSION

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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